1.3GHz bi-directional I^2C bus controlled synthesizer — TSA5511

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I^2C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner
- Analog-to-digital converter
- 8 bus controlled ports (5 for TSA5511T), 4 open collector outputs (bi-directional)
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

DESCRIPTION

The TSA5511 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I^2C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the eight output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5511 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I^2C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δf	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator	3.2	4	4.48	MHz
I_O	open–collector output current	10	–	–	mA
I_O	current limited output current	–	1	–	mA
T_{amb}	operating ambient temperature range	–10	–	80	°C
T_{stg}	storage temperature range (IC)	–40	–	150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5511	18	DIL	plastic	SOT102
TSA5511T	16	SO	plastic	SOT109
TSA5511AT	20	SO	plastic	SOT163

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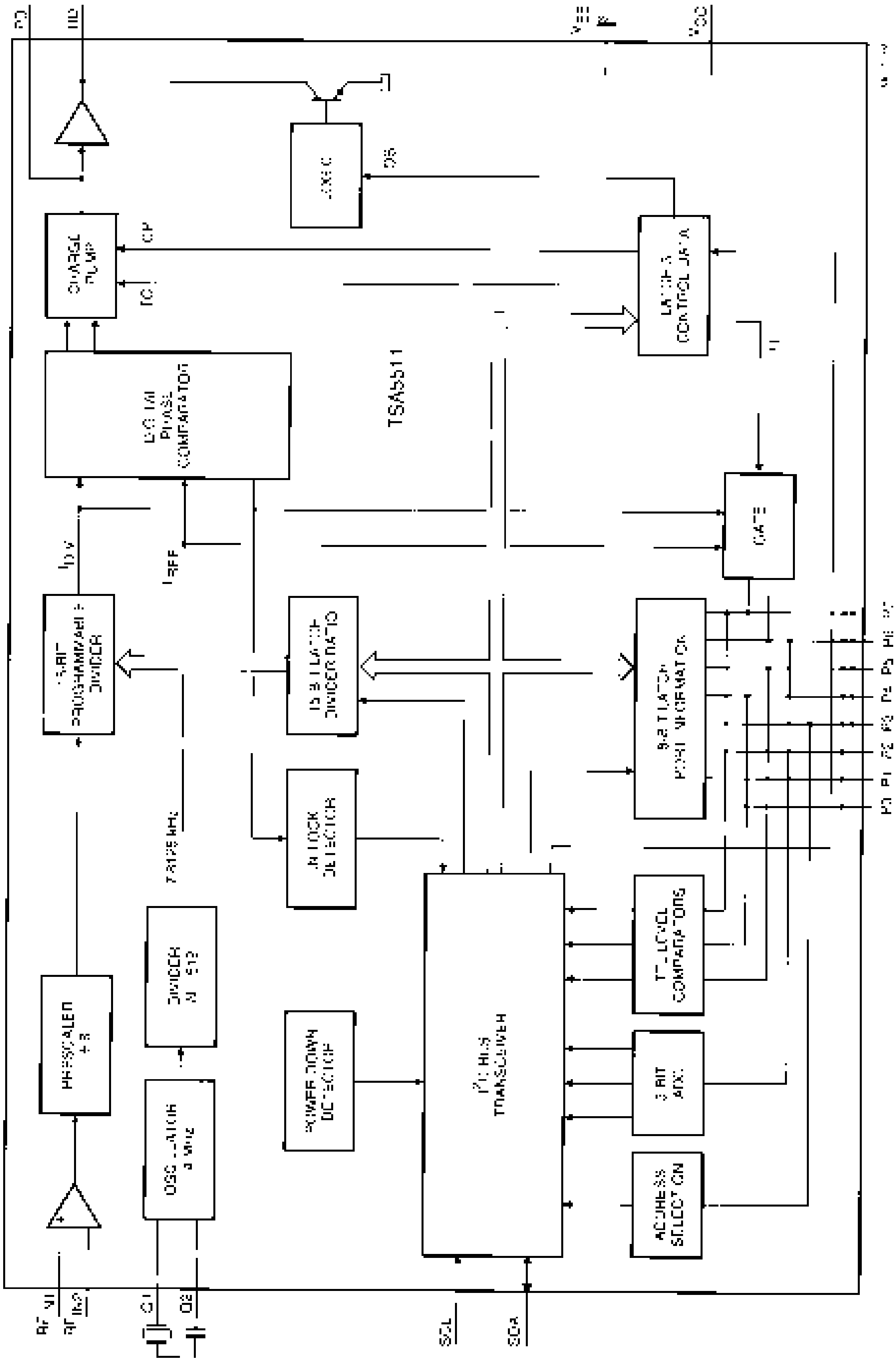


Fig.1 Block diagram.

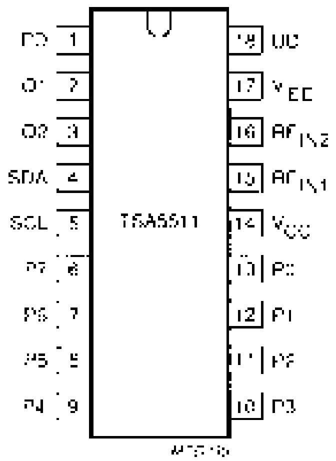


Fig.2 Pin configuration (SOT102).

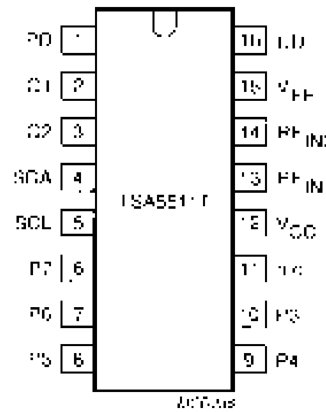


Fig.3 Pin configuration (SOT109).

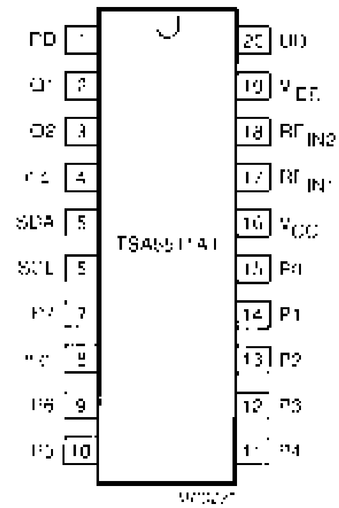


Fig.4 Pin configuration (SOT163).

PINNING

SYMBOL	PIN DIL 18	PIN SO16	PIN SO20	DESCRIPTION
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator input 2
n.c.			4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.			8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
P3	10	10	12	port output/input for address selection
P2	11		13	port output
n.c.		11		not connected
P1	12		14	port output
P0	13		15	port output
V_{CC}	14	12	16	voltage supply
RF_{IN1}	15	13	17	UHF/VHF signal input 1
RF_{IN2}	16	14	18	UHF/VHF signal input 2 (decoupled)
V_{EE}	17	15	19	GND
UD	18	16	20	drive output

FUNCTIONAL DESCRIPTION

The TSA5511 is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode : R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5511. The bus transceiver has an auto-increment facility which permits the programming of the TSA5511 within one single transmission (address + 4 data bytes).

The TSA5511 can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of UHF/VHF signal is first divided by 8 the step size is 62.5 kHz. A 3.2 MHz crystal can offer step sizes of 50 kHz

Table 1 Write data format

	MSB							**LSB**		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	P3	P2*	P1*	P0*	A	byte 5

note

* not valid for TSA5511T

MA1, MA0 programmable address bits (see Table 4)

A acknowledge bit

$N = N14 \times 2^{14} + N13 \times 2^{13} + \ldots + N1 \times 2^{1} + N0$

CP charge-pump current

CP = 0 50 µA

CP = 1 220 µA

P3 to P0 = 1 limited-current output is active

P7 to P4 = 1 open-collector output is active

P7 to P0 = 0 output are in high impedance state

T1 = 1 P6 = f_{ref}, P7 = f_{DIV}

T0 = 1 3-state charge-pump

OS = 1 operational amplifier output is switched off (varicap drive disable)

FUNCTIONAL DESCRIPTION (continued)

READ mode : R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5511 by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5511 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.

A second data byte can be read out of the TSA5511 if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.

The TSA5511 will then release the data line to allow the processor to generate a STOP condition.

When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.

The POR flag (power-on-reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5511 (end of a READ sequence).

Control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked. The bits I2, I1 and I0 represent the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels).

A built-in 5-level ADC is available on I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television as illustrated in the typical application circuit in Fig. 5. The relationship between bits A2, A1 and A0 and the input voltage on port P6 is given in Table 3.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–	byte 2

POR — power-on-reset flag. (POR = 1 on power-on)

FL — in-lock flag (FL = 1 when the loop is phase-locked)

I2, I1, I0 — digital information for I/O ports P7, P5 and P4 respectively

A2, A1, A0 — digital outputs of the 5-level ADC. Accuracy is 1/2 LSB (see Table 3)

MSB is transmitted first.

Address selection

The module address contains programmable address bits (MA1 and MA0) which together with the I/O port P3 offers the possibility of having several synthesizers (up to 3) in one system.

The relationship between MA1 and MA0 and the input voltage I/O port P3 is given in Table 4.

Table 3 A/D converter levels

Voltage applied on the port P6	A2	A1	A0
0.6 V_{CC} to 13.5 V	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V	0	0	0

Table 4 Address selection

MA1	MA0	Voltage applied on port P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_1	charge-pump output voltage	−0.3	V_{CC}	V
V_2	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_4	serial data input/output	0.3	6	V
V_5	serial clock input	−0.3	6	V
V_{5-13}	P7 to P1 I/O voltage	−0.3	+16	V
V_{15}	prescaler input	−0.3	V_{CC}	V
V_{18}	drive output voltage	−0.3	V_{CC}	V
I_5	P7 to P0 output current (open collector)	−1	15	mA
I_4	SDA output current (open collector)	−1	5	mA
T_{stg}	storage temperature range (IC)	−40	+150	°C
T_j	maximum junction temperature		150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j-a}$	from junction to ambient in free air (DIL18)	-	80	K/W
	from junction to ambient in free air (SO16)	-	110	K/W
	from junction to ambient in free air (SO20)	-	80	K/W

CHARACTERISTICS

V_{CC} = 5 V, T_{amb} = 25 °C; unless otherwise specified
All pin numbers refer to DIL 18 version

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Functional range						
V_{CC}	supply voltage range		4.5		5.5	V
T_{amb}	operating ambient temperature range		−10	–	80	°C
f_{CLK}	clock input frequency		64		1300	MHz
N	divider		256	–	32767	
I_{CC}	supply current		25	35	50	mA
f_{XTAL}	crystal oscillator		3.2	4	4.48	MHz
Z_I	input impedance (pin 2)		480	400	–320	Ω
	input level	V_{CC} = 4.5 V to 5.5 V; T_{amb} = −10 to 80 °C; see typical sensitivity curve in Fig. 6				
	f = 80 to 150 MHz		12/ 25	–	300/2.6	mV/dBm
	f = 150 to 1000 MHz		9/−28	–	300/2.6	mV/dBm
	f = 1000 to 1300 MHz		40/−15	–	300/2.6	mV/dBm
R	prescaler input resistance see SMITH chart in Fig. 7		–	50	–	Ω
C	input capacitance		–	2	–	pF
Output ports (current-limited) P0-P3						
I_{LO}	leakage current	V_{12} = 13.5 V	–	–	10	μA
I_{sink}	output sink current	V_{13} = 12 V	0.7	1.0	1.5	mA
Output ports (open collector) P4-P7 (see note 1)						
I_{LO}	leakage current	V_9 = 13.5 V	–		10	μA
V_{OL}	output voltage LOW	I_9 = 10 mA; note 2	–	–	0.7	V
Input P3						
I_{OH}	input current HIGH	V_{OH} = 13.5 V	–	–	10	μA
I_{OL}	input current LOW	V_{OL} = 0 V	−10	–	–	μA
Input ports P4-5, P7						
V_{IL}	input voltage LOW		–	–	0.8	V
V_{IH}	input voltage HIGH		2.7	–	–	V
I_{IH}	input current HIGH	V_6 = 13.5 V			10	μA
I_{IL}	input current LOW	V_6 = 0 V	−10	–	–	μA
Input port P6						
I_{IH}	input current HIGH	V_7 = 13.5 V	–	–	10	μA
I_{IL}	input current LOW	V_7 = 0 V	10	–	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA inputs						
V_{IH}	input voltage HIGH		3.0		5.5	V
V_{IL}	input voltage LOW		–	–	1.5	V
I_{IH}	input current HIGH	V_5 = 5 V, V_{CC} = 0 V; V_5 = 5 V, V_{CC} = 5 V	– –		10 10	μA μA
I_{IL}	input current LOW	V_5 = 0 V, V_{CC} − 0 V; V_5 = 0 V, V_{CC} − 5 V	−10 −10	– –	– –	μA μA
Output SDA (open collector)						
I_{LO}	leakage current	V_4 = 5.5 V	–	–	10	μA
V_4	output voltage	I_4 = 3 mA	–	–	0.4	V
Charge-pump output PD						
I_{1H}	input current HIGH (absolute value)	CP = 1	90	220	300	μA
I_{1L}	input current LOW (absolute value)	CP = 0	22	50	75	μA
V_O	output voltage	in-lock	1.5	–	2.5	V
I_{1leak}	off-state leakage current	T0 = 1	−5	–	5	nA
Operational amplifier output UD (test mode : T0 = 1)						
V_{18}	output voltage	V_{IL} = 0 V		–	100	mV
V_{18}	output voltage when switched-off	OS = 1; V_{IL} = 2 V	–		200	mV
G	operational amplifier current gain; $I_{18}/(I_1 - I_{1leak})$	OS = 0; V_{11} − 2 V; I_{18} = 10 μA	2000	–	–	

Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with a single open-collector port active.

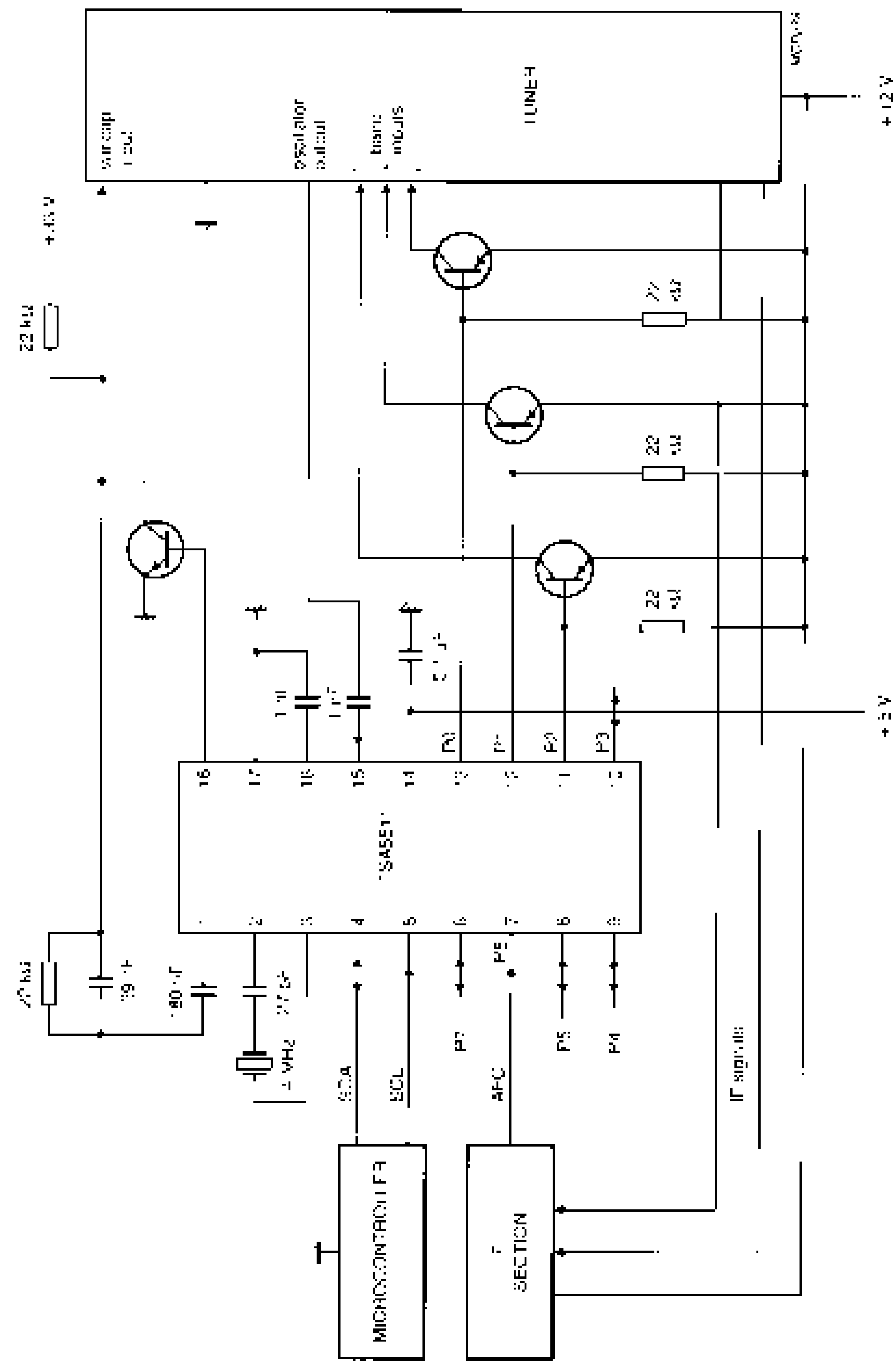


Fig.5 Typical application (DIL18).

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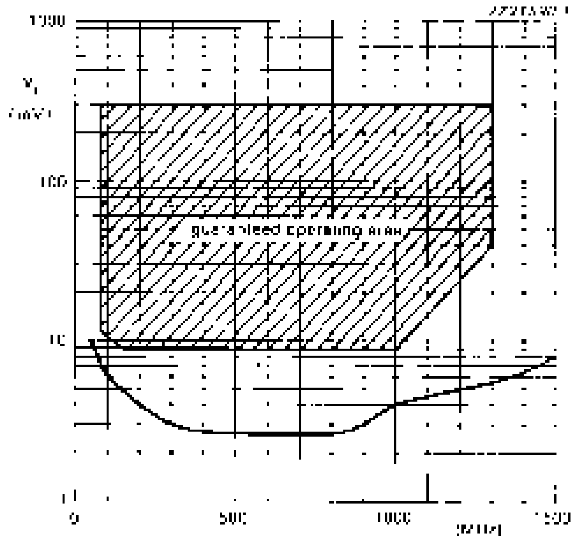


Fig.6 Prescaler typical input sensitivity curve; V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to +80 °C.

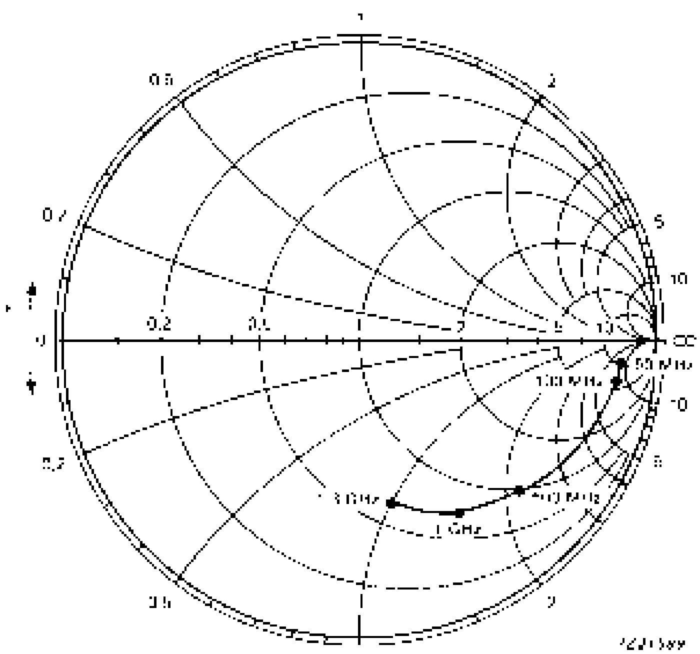


Fig.7 Prescaler Smith chart of typical input impedance; V_{CC} = 5 V, reference value = 50 Ω

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2) / (C1 \times C2)$$

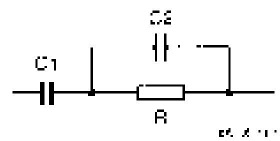


Fig.8 Loop filter.

where:

K_{VCO}	=	oscillator slope (Hz/V)
I_{CP}	=	charge-pump current (A)
K_O	=	4 x 10E6
C1 and C2	=	loop filter capacitors

FLOCK FLAG APPLICATION

- K_{VCO} = 16 MHz/V (UHF band)
- I_{CP} = 220 μA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ± 27.5 kHz.

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	μs
Time span between the loop losing lock and FL-flag resetting	0	128	μs

Purchase of Philips I^{2}C components conveys a license under the Philips' I^{2}C patent to use the components in the I^{2}C system provided the system conforms to the I^{2}C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.